ABSTRACT OF THE DISCLOSURE

A memory circuit device comprising a plurality of memory cells connected to a plurality of bit lines and word lines, an access circuit connected to the plurality of bit lines and word lines to select predetermined memory cells from the plurality of memory cells in response to an address signal, a precharge circuit which precharges the bit lines connected to the memory cells selected by the access circuit at the time of a read mode, a common source line connected to a plurality of selected memory cells selected by the access circuit, a source line potential control circuit to connect the common source line to a ground node at a predetermined timing, and a discharge circuit which discharges the bit lines connected to non-selected memory cells other than the selected memory cells.